

## ***Expert Clock Domain Crossing (CDC) & FIFO Design Techniques***

by

Recognized Verilog & SystemVerilog Guru, Cliff Cummings of Paradigm Works, Inc.

*Cliff Cummings is the only Verilog & SystemVerilog Trainer who helped develop every IEEE & Accellera Verilog, Verilog Synthesis and SystemVerilog Standard.*

### **Course Summary**

#### **Course Description**

Sunburst Design – Expert Clock Domain Crossing & FIFO Design Techniques is a 1-day, expert-level course that teaches multi-clock techniques used in large projects and in FIFO design. These materials are based on Cliff's award-winning, frequently referenced multi-clock and FIFO design papers. The course objective is to introduce engineers to world-class SystemVerilog language capabilities using award-winning materials developed by renowned Verilog & SystemVerilog Guru, Cliff Cummings.

<b>Duration</b>	1 Day
<b>Breakdown</b>	60% Lecture, 40% Lab
<b>Level</b>	Expert
<b>Prerequisites</b>	Fundamental Verilog or SystemVerilog coding training or experience
<b>Online Details</b>	The course delivery can be in-person or virtual (virtual courses are convenient for both U.S. and non-U.S. engineers).

## Course Syllabus

### Half Day #1

#### **Multi-clock Clock Domain Crossing (CDC) Design Techniques using SystemVerilog**

Very advanced design techniques from Cliff's award-winning presentations on the efficient implementation of multi-clock CDC designs. These materials are not specific to SystemVerilog, but solutions are shown using SystemVerilog syntax (advanced techniques that all design engineers should know - the stuff you did not learn in college).

#### **(1) Metastability & synchronizers - synchronizing 1-bit signals**

#### **(2) Passing multiple control signals - synchronizing multi-bit signals or buses**

- (a) Consolidation
- (b) Controlled- multicycle path formulations (MCP)
- (c) FIFO synchronizer
- (d) Gray codes & Gray code counters

#### **(3) Design Partitioning - design & synthesis techniques**

- (a) Naming conventions
- (b) Synthesis scripting & timing analysis issues

#### **(4) Simulation Issues**

- (a) X-propagation issues
- (b) Synopsys command for SDF files
- (c) Multi-SDF files
- (d) ASIC/FPGA vendor cells and models
- (e) Simulation model to expose synchronization problems

#### **(5) LAB: MCP-controlled synchronization**

### Half Day #2

#### **Multi-clock FIFO Design Techniques using SystemVerilog**

Very advanced design techniques from Cliff's award-winning presentations on the efficient implementation of FIFO designs. These materials are not specific to SystemVerilog, but solutions are shown using SystemVerilog syntax (advanced techniques that all design engineers should know - the stuff you did not learn in college).

#### **(1) Multi-clock FIFO design - a large section on FIFO design and FIFO issues**

#### **(2) LAB: 2-clock FIFO**